Claims

[c1] 1. A code implantation process comprising:forming a gate oxide layer on a surface of the substrate;forming a plurality of conductive lines running in a first direction on the gate oxide layer, wherein the conductive lines are covered by a cap layer;forming a dielectric layer over the substrate to cover the cap layer;removing a portion of the dielectric layer until the cap layer is exposed;forming a resist layer with a line/space pattern on the dielectric layer and the cap layer, wherein the line/space pattern extending in a second direction different from the first direction;removing the cap layer not covered by the resist layer; andperforming an ion implantation step to implant dopants into a region not covered by the cap layer.

[c2] 2. The process of claim 1, wherein the conductive lines and the cap layer have an etching selectivity.

[c3] 3. The process of claim 1, wherein the dielectric layer and the cap layer has an etching selectivity.

[c4] 4. The process of claim 1, wherein a material for forming the conductive lines includes polysilicon.

[c5] 5. The process of claim 1, wherein a material for forming the cap layer includes silicon oxide, while a material for forming the dielectric layer is silicon nitride or silicon oxynitride.

[c6] 6. The process of claim 1, wherein a material for forming the dielectric layer includes silicon oxide, while a material for forming the cap layer is silicon nitride or silicon oxynitride.

[c7] 7. The process of claim 1, wherein the first direction is perpendicular to the second direction.

[c8] 8. The process of claim 1, wherein a method for removing a portion of the dielectric layer until the cap layer being exposed is an etching back process or a CMP process.

[c9] 9. The process of claim 1, further comprising removing the resist layer before forming a code mask layer over the substrate.

[c10] 10. The process of claim 1, wherein a material for forming the code mask layer includes silicon oxide or resist.

[c11] 11. A code implantation process for a mask read only memory (MROM), comprising:forming a buried bitline in a substrate;forming a gate oxide layer on a surface of the substrate;forming a wordline on the gate oxide layer and forming a cap layer on a top of the wordline, wherein a stop layer is formed between the wordline and the cap layer;forming a dielectric layer over the substrate to cover the cap layer;removing a portion of the dielectric layer until the cap layer is exposed;forming a resist layer with a line/space pattern on the dielectric layer and the cap layer, wherein the line/space pattern has a first extending direction different to a second extending direction of the cap layer;removing the cap layer not covered by the resist layer;forming a code mask layer over the substrate; andperforming an ion implantation step to implant dopants into a predetermined code channel region by using the code mask layer, the dielectric layer and the remained cap layer as a mask.

[c12] 12. The process of claim 11, wherein the stop layer and the cap layer have an etching selectivity.

[c13] 13. The process of claim 11, wherein the dielectric layer and the cap layer have an etching selectivity.

[c14] 14. The process of claim 11, wherein a material of the wordline is the same as that of the cap layer.

[c15] 15. The process of claim 11, wherein a material of the wordline is different to that of the cap layer.

[c16] 16. The process of claim 11, wherein a material for forming the wordline includes polysilicon.

[c17] 17. The process of claim 11, wherein a material of the cap layer includes polysilicon, while a material of the stop layer is silicon nitride or silicon

oxynitride and a material of the dielectric layer is silicon oxide.

[c18] 18. The process of claim 11, wherein a material of the cap layer includes polysilicon, while a material of the stop layer is silicon oxide and a material of the dielectric layer is silicon nitride or silicon oxynitride.

[c19] 19. The process of claim 11, wherein the first extending direction of the line/space pattern is perpendicular to the second extending direction of the cap layer.

[c20] 20. The process of claim 11, wherein a method for removing a portion of the dielectric layer until the cap layer being exposed is an etching back process or a CMP process.

[c21] 21. The process of claim 11, further comprising removing the resist layer before forming a code mask layer over the substrate.

[c22] 22. The process of claim 11, wherein a material for forming the code layer includes silicon oxide or resist.

[c23] 23. The process of claim 11, wherein forming the wordline, the stop layer and the cap layer further comprises:forming a conductive layer on the gate oxide layer;forming an etching stop layer on the conductive layer;forming a material layer on the etching stop layer; andpatterning the conductive layer, the etching stop layer and the material layer in a direction perpendicular to the buried bitline, to form the wordline, the stop layer and the cap layer on the top of the wordline.

[c24] 24. A contact hole process, comprising:forming a first sacrificial layer over a substrate;forming a first resist layer with a line/space pattern running in a first direction on the first sacrificial layer;removing the first sacrificial layer not covered by the first resist layer;removing the first resist layer;forming a second sacrificial layer over the first sacrificial layer;removing a portion of the second sacrificial layer until the first sacrificial layer is exposed;forming a second resist layer with a line/space pattern on the second and first sacrificial layers, wherein the line/space pattern runs in a second direction;removing the second sacrificial

layer not covered by the second resist layer.

[c25] 25. The process of claim 24, wherein the first sacrificial layer and the second sacrificial layer have an etching selectivity.

[c26] 26. The process of claim 24, wherein a material for forming the first sacrificial layer includes oxide, nitride, silicon oxynitride and BPSG.

[c27] 27. The process of claim 24, wherein a material for forming the second sacrificial layer includes oxide, nitride, silicon oxynitride and BPSG.

[c28] 28. The process of claim 24, wherein a method for removing a portion of the second sacrificial layer until the first sacrificial layer being exposed is an etching back process or a CMP process.